REMARKS

The Office Action dated January 14, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicants appreciate the allowance of claims 1-4.

Claims 5 and 6 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 5-8 are pending in the present application and are respectfully submitted for consideration.

Claims 5 and 6 were rejected under 35 U.S.C. § 112, second paragraph, as failing to set forth the subject matter, which Applicants regard as their invention. Claims 5 and 6 have been amended to more particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention. In particular, claims 5 and 6 have been amended to recite the subject matter of a PPL clock which is an exemplary embodiment of the present invention. Therefore, Applicants submit that the present application is in compliance with US patent practice.

Claims 5 and 7-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yokogawa et al. (U.S. Patent No. 4,872,155, "Yokogawa"). Applicants respectfully submit that each of claims 5 and 7-8 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 5 recites a method for controlling a clock switching circuit comprising the steps of receiving a basic clock signal from an outside, receiving a PLL clock signal

generated by a PLL circuit based on the basic clock signal, the PLL clock signal being faster than the basic clock, counting a number of the PLL clock signal after inhibiting outputting the basic clock signal, and outputting the PLL clock signal after the number of the PLL clock signal which is a predetermined number.

Claim 7 recites a clock signal switching circuit that switches an output from a basic clock to a fast clock. The clock signal switching circuit comprises a PLL circuit that generates the fast clock whose frequency is more than twice as much as a frequency of the basic signal, and an inhibiting circuit that inhibits the fast clock by a time when the basic clock disappears in the output in the case of switching the output from the basic clock to the fast clock.

Claim 8 recites a clock signal switching circuit that switches an output from a basic clock to a fast clock. The clock signal switching circuit comprises a PLL circuit that generates the fast clock whose frequency is more than twice as much as a frequency of the basic signal, and an inhibiting circuit that inhibits the fast clock within a term which depends on a difference between the frequency of the basic clock and the frequency of the fast clock in the case of switching the output from the basic clock to the fast clock.

Accordingly, at least one of the essential features of the present invention is the steps of "counting a number of the basic clock signal after inhibiting outputting the basic clock signal; and outputting the PLL clock signal after the number of the basic clock signal which is a predetermined number." As such, the present invention results in the

advantage of properly switching asynchronous clocks having a large difference in frequency when disconnecting or connecting an interface cable with a hot-plug function.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 5, 7 and 8, and therefore fails to provide the advantages that are provided by the present application.

Yokogawa discloses a recording-reproducing clock generator circuit that generates a reproduced clock having a predetermined frequency from a read out signal including such pulses that the interval between two successive pulses thereof at a predetermined length is to be used as a synchronizing signal region. The circuit of Yokogawa generates a reference clock of a predetermined frequency, generates a first sync signal detection signal when the distance between two successive pulses in the input signal measured by means of the clock pulses is equal to a predetermined reference value, separates a clock edge pulse from the input signal by using the first sync signal detection signal, and generates the reproduced clock having the predetermined frequency and synchronized with the separated clock edge pulse.

Applicants respectfully submit that each and every element recited within claim 5, 7 and 8 is neither disclosed nor suggested by Yokogawa. In particular, Applicants submit that the clock switching circuit and the method of controlling thereof as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the following limitations as forth below.

Claim 5:

"counting a number of the basic clock signal after inhibiting outputting the basic clock signal; and
outputting the PLL clock signal after the number of the basic clock signal which is a predetermined number."

Claim 7:

"an inhibiting circuit that inhibits said fast clock by a time when said basic clock disappears in said output in the case of switching said output from said clock to said fast clock."

Claim 8:

"an inhibiting circuit that inhibits said fast clock within a term which depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock."

In Yokogawa, the clock edge selector circuit 21 in Fig. 10 switches between the clock edge pulse generated by the gate pulse c via AND gate 18 or the clock edge pulse generated by the gate pulse j via the AND gate 19, depending on the detection signal h. However, the clock edge pulses are generated from the same pulse a by employing the different gate pulses c and j. In Yokogawa, the clock f from the oscillator 15 and the clock e from PLL are employed to generate the gate pulses c and j. Therefore, Yokogawa is irrelevant to the present invention, and that Yokogawa fails to disclose or suggest each and every limitation recited in claims 5, 7 and 8 of the present application.

In view of the above, Applicants respectfully submit that each of claims 5-8 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 5-8 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108066-00018.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (2 months)